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Vertically integratable circuit and method for producing same

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This invention relates to a vertically integratable circuit and a method for producing same.

Vertically integratable circuits refer to semiconductor circuits produced by planar technology which are disposed vertically one above the other in several levels, resulting in three-dimensional circuits. The single components and circuit elements of the different levels are electrically interconnected by vertical contacts. This permits higher packing density to be attained compared to two-dimensional circuits, i.e. circuits in only one level. Vertical integration also offers advantages in terms of security since especially sensitive circuit elements can be disposed in levels or layers surrounded on both sides by at least one further level or layer with active components.

In the production of the three-dimensional circuits, in particular the vertical contacts deviate from known technologies since the single vertically integratable circuits are produced by known and readily controllable planar technology. Several methods have become known for producing the vertical contacts.

One known method is based on depositing polycrystalline silicon on a finished component layer and recrystallizing it. Further components can be fabricated in the recrystallized layer. The disadvantage of this method is that the high temperatures during recrystallization can change the properties of the finished active components of the lower level. Furthermore, the serial processing of the vertically integrated overall circuit results in an accordingly longer turnaround time for production.

In another known method it is provided that the single vertically integratable circuits or levels of circuits are produced separately on different substrates. Substrates with single circuit levels are then thinned, provided with front side and backside contacts and connected vertically by a bonding method. The disadvantage of this method is that the front side and backside contacts are produced partly using materials not readily usable in known semiconductor manufacturing processes.

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DE 44 33 845 A1 discloses a method for producing a three-dimensional integrated circuit wherein two finished substrates or single circuits are

interconnected. For vertical electric connection of the circuits contained on both substrates, further process steps are performed to produce a metalization after connecting the two substrates one of which was thinned. The disadvantage of the known method is that completely processed substrates must be made available and additional process steps are required for producing the vertical electric connection.

The problem of the present invention is thus to state a vertically integratable circuit and a method for producing same that manages with fewer process steps.

B3 ~~This problem is solved by the features of the independent claims.~~

It is assumed that the vertical electric contacts are produced using process steps in the production of the vertically integratable circuit itself. This simplifies the sequence of production for vertically integratable circuits and thus the three-dimensional integrated circuit as a whole, thereby optimizing plant running times since process steps are saved. Because finished substrates are no longer the starting point for producing the vertical electric connections, an improved yield is moreover obtained since no process steps which could in particular change the already produced active circuit elements, such as steps with high process temperatures, are necessary any longer after production of the circuit elements.

B4 Further advantages of the invention will result from the following exemplary description with reference to figures, in which:

Figure 1 shows different process steps of a method for producing vertically integratable circuits; and

Figure 2 shows an embodiment of an electrically conductive connection for vertical integration of circuits.

Figure 1 shows the sequence of process steps in the production of vertically integratable circuits.

B5 Figure 1*a* shows substrate 1, 2 in which insulating layer 3 is hidden. Substrate 1, 2 can consist e.g. of silicon, insulating layer 3 e.g. of silicon dioxide. Such substrates are known and referred to as SOI (silicon on insulator) substrates. Gaps 4 are formed, e.g. by etching, in substrate 1 above insulating layer 3 as far as insulating layer 3 and surrounding bars 5 in substrate 1. Bars 5 are so dimensioned that they can

be completely oxidized in a following process step. Gaps 4 and bars 5 are so dimensioned that their surface area suffices for receiving contacts for vertical integration and for forming an insulation for said contacts. Simultaneously with gaps 4, alignment marks (not shown) can also be etched to be later used for aligning the circuits or the substrate for vertical integration.

Figure 1*b* shows SOI substrate 1, 2, 3 after further process steps. Differently doped tubs 6 and oxide layers 8 and 9 have been produced. Doped tubs 6 as well as field oxide 8 and gate oxide 9 later form the active components of the vertically integratable circuit. Their production and mode of functioning is known and therefore need not be described, especially since it is not of importance for understanding the present invention. After oxidation, e.g. high-temperature oxidation, there is at the place of gaps 4 and bars 5 of Figure 1*a* an oxide that is part of field oxide 8 and reaches as far as insulating layer 3. During oxidation one must make sure the field oxide is free from cavities and the resulting surface is as planar as possible.

Figure 1*c* shows substrate 1, 2, 3, after completion of the components, e.g. by incorporation of different doping materials 11 and 12 or by application of polycrystalline silicon 10. To permit further processing, insulating or planarizing layer 7, e.g. of photoresist or polyimide, has furthermore been applied.

Figure 1*d* shows gaps 13 and 14 formed for a first metalization level, which can be produced for example by etching and are known as vias. Gaps 14 are used for connecting a component, a transistor here; gaps 13 are intended for later vertical integration.

Figure 1*e* shows through metalizations 15 and 16 formed for the first metalization level which fill vias 13 and 14 of Figure 1*d*. In a subsequent process step (not shown) a metalization is applied to the surface of planarizing layer 7 for connecting through metalizations 15 and 16. Aluminum is normally used for the metalizations.

Further metalization levels can follow, whereby an insulating layer, e.g. of silicon dioxide, is applied after each metalization level. Besides the shown and

described production of gaps 13 and through metalizations 15 for the contacts for vertical integration in the first metalization level, they can also be provided in other metalization levels. After production of all metalization levels, different cover layers are usually applied, such as a passivation layer, oxide layer and planarizing layer.

Figure 1*f* shows substrate 1, 3 after thinning. Lower layer 2 of substrate 1, 2, 3, as shown in the preceding figures, was removed e.g. by an etching operation. The shown use of a substrate with hidden insulating layer 3 proves especially advantageous since the latter serves as an etching stop. But it is also fundamentally possible to use other substrates. However, the latter must be insulated on the backside e.g. by oxide deposition after thinning. For handling the substrate during thinning and subsequent processing, the substrate can be applied with its processed surface 1 to a handling wafer from which it is detached after complete processing. The substrate is thinned as far as oxide 8 in this case. In both cases it can also be provided that through metalization 15 is formed up to the end of oxide 8, i.e. the previous etching is accordingly deep.

Figure 1*g* shows processed substrate 1, 3 wherein gaps 17 have been etched from backside 3 at the places of the contacts for vertical integration. The etching, which can be done wet-chemically for example, reaches as far as through metalizations 15.

Figure 1*h* shows final backside metalization 18 of substrate 1, 3. Backside metalization 18 is performed so as to create contacts 15, 18 required for vertical integration, i.e. backside metalization 18 is interrupted at the places of through metalization 15, as shown in Figure 1*h*. Finally, cover layers can also be applied to the backside metalization, as described above for the front side of the substrate. As described above, oxide 8 was dimensioned at the place of contact for vertical integration 15, 18 so as to completely enclose contact for vertical integration 15, 18 for electric insulation.

The circuits or substrates for vertical integration produced by the above described method are then joined together for example with backside metalizations 18, the abovementioned alignment marks being used for alignment. Connection of

more than two substrates is possible if the contacts for vertical integration are also guided onto the surface of processed substrate 1. In this case it might be necessary to use infrared technologies for alignment since the alignment marks may be covered by the vertical integration.

For producing an electric connection between the contacts for vertical integration in different levels, i.e. different substrates, backside metalizations or metalizations on the surfaces of the processed substrates can be provided which melt or begin to melt at low temperatures to yield a reliable electric connection. Places on the surfaces, on the front side or backside of the substrate, with contacts for vertical integration must furthermore not be covered by the abovementioned cover layers so that an electric connection can be made. For this purpose such places can either be left out during production of the cover layers, or for example be etched free after production of the cover layers.

For vertical integration it can be provided that whole substrates provided with contacts for vertical integration are connected in the described way. It is also possible to divide the substrates into single circuits and vertically integrate single circuits. Before vertical integration the single circuits can be tested and faulty ones rejected. Another possibility is vertical integration of single circuits on circuits of a whole substrate and subsequent division of the substrate. This possibility also permits prior functional testing of both the single circuits and the circuits on the substrate.

Besides the above-described process for producing vertically integratable circuits on the basis of a silicon substrate, it is also possible to use the inventive method for processes based on other semiconductor materials.

Figure 2 shows an advantageous embodiment of an inventive contact for vertical integration. In addition to contact for vertical integration 15, 18 described in connection with Figure 1, further metalization 19 is provided within insulating oxide 8. Metalization 19 is e.g. of annular design and completely surrounds the metalization of contact for vertical integration 15. Further, annular metalization 19 is electrically connected by the metalization applied to the surface in a later process

step so that it is grounded in operation. This permits the signal flow through vertical contact 15, 18 to be shielded. Then the signal flow through the contact for vertical integration cannot be evaluated from one of the end faces of the substrate in case the contact for vertical integration is located near one of the end faces of the substrate.